ABSTRACT

A circuit provides latched data in a domino circuit environment. The circuit receives a pair of input signals that are either in complementary logic states, which is data, or in the same logic state, which is the reset condition. The circuit responds to the complementary logic states by providing intermediate signals and output signals in corresponding complementary logic states. The intermediate logic states are latched by cross-coupled clocked inverters prior to the pair of signals switching from data to reset. The intermediate signals are thus latched in the complementary logic states that correspond to data even after the pair of input signals have returned to reset. The output signals are also thus provided in complementary logic states that correspond to data prior to the input signals being reset.